IN THE SPECIFICATION

Please amend the abstract as follows:

ABSTRACT OF THE DISCLOSURE

~~**Image Processor and Method of Processing Images**~~

An image processor ~~is~~ arranged in operation to generate an interpolated video signal from a received video signal representative of an image. The image processor comprises an adaptable register store comprising a plurality of register elements and is coupled to a control processor which is operable to receive the video signal and to provide pixels of the received video signal, under control of the control processor[[,]] to an interpolator, selected register elements being connected to the interpolator to provide the pixels of the received video signal for interpolation, each of the register elements being arranged to store a pixel of the received video signal and each is connected to a plurality of other register elements and is configurable under control of the control processor to feed the pixel stored in the register element to one of the plurality of other register elements in accordance with a temporal reference and the interpolator being coupled to the adaptable register store. ~~and is arranged in operation to generate the interpolated video signal by interpolating the pixels provided by the adaptable register store. The control processor controls in operation the adaptable register store to provide pixels to the interpolator to interpolate parts of the image in both vertical and horizontal directions. Performing diagonal interpolation can substantially reduce ringing effects and resolution loss on diagonal edges of an image. In order to interpolate a part or all of the image in both the vertical~~

~~and horizontal directions, the adaptable shift register may have a plurality of register elements, selected register elements being connected to the interpolator to provide the pixels of the received video signal for interpolation, each of the register elements being arranged to store a pixel of the received video signal and each being connected to a plurality of other register elements and configurable under control of the control processor to feed the pixel stored in the register element to one or other of the other shift registers in dependence upon a temporal reference.~~

~~[Fig 10]~~